TE/ sem VI/ (EXTC CBSGS)/ Digital Communications/ NOV 2015

Q.P.No. : **6278**

Duration: 3 Hrs Total Marks: 80

N.B: Question No 1 is compulsory.
Attempt any three questions out of remaining five.
All questions carry **equal** marks
Assume Suitable data, if required and state it clearly.

Q1) (20)

a) Describe in brief four types of Trade-Offs that can be accomplished by using Error correcting code.
b) How is signal bandwidth spread in spread spectrum modulation?
c) What is Entropy of an information source? When is entropy maximum?
d) What is gram Schmitt orthogonalization procedure? Explain?
e) Distinguish between Matched filter and Correlator.

Q2) a) Consider a DMS S = (S_1, S_2, S_3....S_7)with following message probabilities (10)

S_i	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$P(s_i)$	0.40	0.25	0.15	0.10	0.05	0.03	0.02

Encode the source using Huffman algorithm. Find the average code length and efficiency.

b) Explain the necessity of line codes for data transmission. State different types of line codes. Plot power spectral density of NRZ signal. (10)

Q3) a) State and explain maximum likelihood decision rule. Explain the function of correlator receiver. (10)

b) *Derive the expression for error probability of BPSK system with coherent detection.* (10)

Q4) a) *Draw and explain the block diagram of OQPSK transmitter. Sketch the waveforms at the* output of each block of the transmitter. (10)

b) Consider a (7, 4) code whose generator matrix is (10)

$$G = \begin{matrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{matrix}$$

1) Find **H**, the Parity – Check matrix of the code.
2) Compute the syndrome for the received vector 1 1 0 1 1 0 1.Is this a valid code vector?

Q5)a) Design Encoder for an (8,5) cyclic code with generator $g(x) = 1+x+x^2+x^3$.Use this encoder to find the code word for the message (10101) in systematic form. (10)

b) Draw the state Diagram and Tree diagram for L= 3, rate $=\frac{1}{3}$ convolution encoder generated by $g_1(x) = x+ x^2$, $g_2(x) = 1+x$, $g_3(x) = 1+x+x^2$. (10)

Q6) a) What are two basic types of spread spectrum systems? Explain the basic principle of each of them. (10)

b) Explain in detail 16-QAM transmitter and receiver system .Draw and explain signal constellation diagram for 16-QAM. (10)

EXTC/SEM-VI (CBSGS)/Diskrit Time Signal Processing/
Nov. Dec 2015

QP Code : **6320**

(3 Hours) [Total Marks :80

N.B. : (1) Question no. **1** is **compulsory.**
(2) Solve any **three** questions from remaining **five questions.**
(3) In all **four** questions to be attempted.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) The first five points of eight point DFT of real valued signal are {0.25, 0.125 -j0.3018, 0, 0.125-j0.0150, 0}. Determine the remaining three points. 20

(b) Sketch the frequency response and identify the following filters based on their passband

(i) $h(n)=\left\{1,-\frac{1}{2}\right\}$

(ii) $H(z)=\frac{z^{-1}-a}{1-az^{-1}}$

(c) What is multirate DSP? State its applications

(d) An analog filter has transfer function

$$H(s)=\frac{S+0.1}{(S+0.1)^2+16}$$

Determine transfer function of digital filter using bilinear transformation.

The digital filter should have a specification of $\omega_r=\pi/2$

2. (a) Compute DFT of sequence $x(n)=\{1, 2, 2, 2, 1, 0, 0, 0\}$ using DIT-FFT algorithm. 10

(b) Explain the effects of coefficients quantization in FIR filters. 10

3. (a) Implement a two stage decimatior for the following specification: 10
Sampling rate of the input signal = 20,000Hz,
Decimating factor M = 100,
Passband = 0 to 40Hz,
Passband ripple = 0.01,
Transition band = 40 to 50Hz,
Stop band ripple = 0.002

(b) (i) If $x(n)=\{1+2j, 3+4j, 5+6j, 7+8j\}$. Find DFT X(k) using DIF-FFT algorithm. 10

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4. (a) Explain upsampling process in detail and derive for input-output relationship in time domain and frequency domain. 10

(b) Obtain cascade and parallel realization structures for the system described by $y(n) = -0.1y(n-1) + 0.72y(n-2) + 0.7\,x(n) - 0.252\,x(n-1)$ 10

5. (a) Design a FIR digital filter using window method for following specifications. 10

$$H(e^{j\omega}) = e^{-j3\omega} \quad 0 \le |\omega| \le \frac{3\pi}{4}$$
$$= 0 \qquad \text{otherwise}$$

Use Hamming window of length 7

(b) Design a digital low pass IIR Butterworth filter for the following specification 10

Passband ripple	:	≤ 1 dB
Passband edge	:	4 KHz
Stopband attenuation	:	40 dB
Stop edge	:	8 KHz
Sampling Rate	:	24 KHz

Use bilinear transformation

6. (a) Write a short note on: 10

(i) Dual tone multi frequency signal detection

(ii) Different methods for digital signal synthesis

(b) Determine the zeros of the following FIR systems and indicate whether the system is minimum phase, maximum phase or mixed phase. 10

(i) $H_1(z) = 6 + z^{-1} - 6z^{-2}$

(ii) $H_2(z) = 1 - z^{-1} - 6z^{-2}$

(iii) $H_3(z) = 1 - \frac{5}{2}z^{-1} - \frac{3}{2}z^{-2}$

(iv) $H_4(z) = 1 - \frac{5}{2}z^{-1} - \frac{2}{3}z^{-2}$

Comment on stability of minimum and maximum phase system

Computer communication & Telecom n/w's, EXTC, Nov/Dec-2015

EXTC VI (CBSGS)

QP Code : 6363

(3 Hours) [Total Marks :80

N.B. : (1) Question **No.1** is **compulsory**
(2) Write any **three** question from Q.2 to Q.6.
(3) Draw neat diagram if necessary.

1. Solve following 20
   (a) Compare between pure ALOHA and Slotted ALOHA
   (b) Explain working principle of selective repeat ARQ
   (c) What is the use of subnetwork in IP addressing
   (d) What is bit and byte stuffing explain with example.

2. (a) Discuss various scheduling methods used in MAC 10
   (b) Explain need of fragmentation and field related to fragmentation in IP datagram 10

3. (a) Solve the following related of IP datagram
      (a) Which field shows number of hop count 10
      (b) If HLEN value is 5 and length of data is 24 bytes. Calculate option
      (c) What are differentiate services?
      (d) Packet version of 010 is discarded. Justify.
   (b) Draw and explain connection establishment using 3 way handshaking in TCP. 10

4. (a) What is DSL and HFC? Describe in brief 10
   (b) What is IEEE 802.11? Explain features of IEEE 802.11. Draw the architecture of IEEE 802.11 10

5. (a) What do you mean by decentralized peer to peer file sharing? How it is different from centralized system. 5
   (b) What are the components of ATM? Explain in brief.
   (c) What is the role of ICMP protocol? Explain the error messages of ICMP 5 10

6. (a) An ISP are granted a block of address starting with 127.60.4.0/20. The ISP wants with each organization receiving 8 address only Design subblock and give the slash notation for each subblock. 10
   (b) Which protocol gives mapping of name with IP address? Explain working of such protocol with different records. 10

TE/Sem-VII. CBSGS/EXTC/- VLSI Design/ Nov'15.

QP Code : 6491

(3 Hours) **[Total Marks : 80**

N.B.: (1) **Question No. 1** is compulsory. Solve any **three** from the remaining **five** questions.
(2) Figures to right indicate full marks.
(3) Assume suitable data if required and mention the same in the answer sheet.

1. Solve **any five** from the following **20**
   a) Explain Level 1 and Level 2 MOSFET model used in circuit simulator.
   b) In 2 input CMOS NAND gate all PMOS transistors have $\left(\frac{W}{L}\right)_p = 20$ and all NMOS transistors have $\left(\frac{W}{L}\right)_n = 10$. Draw its equivalent CMOS inverter and find size of PMOS and NMOS transistor in the equivalent inverter circuit.
   c) What are advantages & disadvantages of dynamic logic circuit.
   d) Why sense amplifier is used in memory circuit. Explain its working.
   e) How low power circuit is designed through voltage scaling.
   f) Explain hot carrier effect in short channel MOSFET.

2. a) Compare resistive load inverter, saturated load inverter and CMOS inverter on the basis of Noise margins, power dissipation, area and delay. **10**
   b) Draw 2 input CMOS NOR gate and using equivalent inverter approach and derive expression for V_{IL}, V_{IH}, V_{OL} and V_{OH}. **10**

3. a) Design clocked D-FF and implement using standard CMOS logic style. **10**
   b) Draw layout of six transistor CMOS SRAM using lambda rule. **10**

4. a) Explain 4-bit x 4-bit array multiplier with the help of necessary hardware for the generation and addition of partial product. **10**
   b) Why ESD protection is required for CMOS chips. Explain various techniques of ESD protection. **10**

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5. a) Implement $y = \overline{A(D+E)+BC}$ using 10
   i) Static CMOS style
   ii) Pseudo NMOS logic style
   iii) Dynamic logic style
   iv) Transmission Gate logic

   b) What are different types of MOSFET scaling? Explain advantages and disadvantages of each using appropriate equations. 10

6. Write short notes on **any four** 20
   i) 3T-DRAM cell
   ii) Clock distribution in VLSI system
   iii) Barrel shifter
   iv) C^2MOS logic style
   v) 1-bit shift register